CLAIMS

1. A method of fabricating a semiconductor device comprising:

forming a first dielectric layer over a base substrate;

forming a damascene trench in said first dielectric layer, said damascene trench having a gate area and a local interconnect area;

forming a gate oxide layer on said base substrate within said gate area of said damascene trench;

filling said damascene trench with a conductive material; and,

removing said first dielectric layer to define a damascene gate structure and a damascene local interconnect structure.

2. A method of fabricating a semiconductor device according to claim 1, further comprising forming an isolation trench in said base substrate before said first dielectric layer is formed.

3. A method of fabricating a semiconductor device according to claim 2, wherein at least a portion of said damascene trench at least partially overlies said isolation trench.

4. A method of fabricating a semiconductor device according to claim 2, wherein said isolation trench formation comprises:

depositing a pad oxide layer over said base substrate;

depositing a nitride layer over said pad oxide layer;

forming a mask over said nitride layer;

etching through portions of said nitride layer and said pad oxide layer and etching into said base substrate defining an isolation trench opening in said base substrate;

stripping away said mask;

filling said isolation trench opening with a dielectric material; and,

removing said pad oxide layer and said pad oxide layer.

5. A method of fabricating a semiconductor device according to claim 1, wherein said first dielectric layer formation comprises depositing a conformal inter-layer dielectric material over said base substrate.

6. A method of fabricating a semiconductor device according to claim 1, wherein said damascene trench formation comprises:

forming a patterned mask over said first dielectric layer;

etching through said first dielectric layer to said base substrate in areas defined by said patterned mask; and,

stripping said patterned mask from said first dielectric layer.

7. A method of fabricating a semiconductor device according to claim 1, further comprising providing at least one implant within said base substrate through said damascene trench.

8. A method of fabricating a semiconductor device according to claim 1, wherein said gate oxide layer formation comprises:

growing an oxide layer on said base substrate;

forming a patterned mask over said semiconductor device, said pattern arranged to expose at least a portion of said oxide layer within said local interconnect area;

etching away the exposed portion of said oxide layer; and,

stripping said patterned mask from said semiconductor device.

9. A method of fabricating a semiconductor device according to claim 8, further comprising providing a contact implant within said base substrate through said damascene trench prior to stripping said patterned mask.

10. A method of fabricating a semiconductor device according to claim 1, wherein said conductive material comprises a polysilicon material.

11. A method of fabricating a semiconductor device according to claim 10, further comprising forming a silicide layer over said polysilicon material within said gate area of said damascene trench.

12. A method of fabricating a semiconductor device according to claim 10, further comprising forming a silicide layer between said base substrate and said polysilicon within said local interconnect area of said damascene trench.

13. A method of fabricating a semiconductor device according to claim 12, further comprising removing said polysilicon material from said local interconnect area of said damascene trench, forming said silicide layer within said local interconnect area, and refilling said damascene trench with polysilicon.

14. A method of fabricating a semiconductor device according to claim 1, further comprising forming lightly doped drain regions in said base substrate after removing said first dielectric layer, said lightly doped drain regions formed within said base

substrate adjacent to said damascene gate structure and said damascene local interconnect structure.

15. A method of fabricating a semiconductor device according to claim 1, further comprising forming spacers against the vertical walls of said damascene gate structure and said damascene local interconnect structure.

16. A method of fabricating a semiconductor device according to claim 1, further comprising:

forming lightly doped drain regions in said base substrate after removing said first dielectric layer, said lightly doped drain regions formed within said base substrate adjacent to said damascene gate structure and said damascene local interconnect structure;

forming spacers against the vertical walls of said damascene gate structure and said damascene local interconnect structure; and,

forming doped source/drain regions in said base substrate after forming said spacers such that said base substrate is doped more deeply into said base substrate adjacent to said spacers than into said base substrate underneath said spacers.

17. A method of fabricating a semiconductor device comprising:

forming a first dielectric layer over a base substrate;

forming at least one damascene trench in said first dielectric layer, each damascene trench having at least one gate area and at least one local interconnect area;

forming a gate oxide layer on said base substrate within said gate areas of each damascene trench;

filling each damascene trench with a conductive material; and,

removing said first dielectric layer to define at least one damascene gate structure and at least one damascene local interconnect structure.

18. A method of fabricating a semiconductor device according to claim 17, wherein said at least one gate area and said at least one local interconnect area are formed in a single process comprising:

forming a patterned mask over said first dielectric layer;

etching through said first dielectric layer to said base substrate in areas defined by said patterned mask; and,

stripping said patterned mask from said first dielectric layer.

19. A method of fabricating a semiconductor device according to claim 17, further comprising providing at least one contact implant within said base substrate through said damascene trench.

20. A method of fabricating a semiconductor device according to claim 17, wherein said gate oxide layer formation comprises:

growing an oxide layer on said base substrate;

forming a patterned mask over said semiconductor device, said pattern arranged

to expose at least a portion of said oxide layer within each local interconnect area;

etching away the exposed portion of said oxide; and,

stripping said patterned mask from said semiconductor device.

21. A method of fabricating a semiconductor device according to claim 17, further comprising forming lightly doped drain regions in said base substrate after removing said first dielectric layer.

22. A method of fabricating a semiconductor device according to claim 17, further comprising:

forming lightly doped drain regions in said base substrate after removing said first dielectric layer, said lightly doped drain regions formed within said base substrate adjacent to said at least one damascene gate structure and said at least one damascene local interconnect structure;

forming spacers against the vertical walls of said damascene gate structure and said damascene local interconnect structure; and,

forming doped source/drain regions in said base substrate after forming said spacers such that said base substrate is doped more deeply into said base substrate adjacent to said spacers than into said base substrate underneath said spacers.

23. A method of fabricating a semiconductor device comprising:

forming at least one isolation trench;

forming a first dielectric layer over a base substrate;

forming at least one damascene trench in said first dielectric layer, each damascene trench having at least one gate area and at least one local interconnect area, said damascene trench formed such that at least a portion of at least one of said local interconnect areas overlies at least a portion of at least one isolation trench;

forming a gate oxide layer on said base substrate within said gate areas of each damascene trench;

filling each damascene trench with a conductive material; and,

removing said first dielectric layer to define at least one damascene gate structure and at least one damascene local interconnect structure.

24. A method of fabricating a semiconductor device according to claim 23, wherein said at least one gate area and said at least one local interconnect area is formed in a single process comprising:

forming a patterned mask over said first dielectric layer;

etching through said first dielectric layer to said base substrate in areas defined by said patterned mask; and,

stripping said patterned mask from said first dielectric layer.

25. A method of fabricating a semiconductor device according to claim 23, further comprising providing at least one contact implant within said base substrate through said damascene trench.

26. A method of fabricating a semiconductor device according to claim 23, wherein said gate oxide layer formation comprises:

growing an oxide layer on said base substrate;

forming a patterned mask over said semiconductor device, said pattern arranged to expose at least a portion of said oxide layer within each local interconnect area;

etching away the exposed portion of said oxide layer; and,

stripping said patterned mask from said semiconductor device.

27. A method of fabricating a semiconductor device according to claim 23, further comprising forming lightly doped drain regions in said base substrate after removing said first dielectric layer.

28. A method of fabricating a semiconductor device according to claim 23, further comprising:

forming lightly doped drain regions in said base substrate after removing said first dielectric layer, said lightly doped drain regions formed within said base substrate adjacent to said at least one damascene gate structure and said at least one damascene local interconnect structure;

forming spacers against the vertical walls of said damascene gate structure and said damascene local interconnect structure; and,

forming doped source/drain regions in said base substrate after forming said spacers such that said base substrate is doped more deeply into said base substrate adjacent to said spacers than into said base substrate underneath said spacers.

29. A method of fabricating a semiconductor device comprising:

forming a first dielectric layer over a base substrate;

forming a first damascene trench in said first dielectric layer, said first damascene trench having at least one gate area;

forming a second damascene trench in said first dielectric layer, said second damascene trench having at least one local interconnect area;

forming a gate oxide layer on said base substrate within said gate areas of said first damascene trench;

filling said first and second damascene trenches with a conductive material; and,

removing said first dielectric layer to define at least one damascene gate structure and at least one damascene local interconnect structure.

30. A method of fabricating a semiconductor device according to claim 29, further comprising forming at least one isolation trench in said base substrate before said first dielectric layer is formed.

31. A method of fabricating a semiconductor device according to claim 30, wherein at least a portion of said second damascene trench at least partially overlies at least one of said isolation trenches.

32. A method of fabricating a semiconductor device according to claim 29, wherein said first and second damascene trenches are formed in a single process comprising:

forming a patterned mask over said first dielectric layer, said patterned mask defining said first and second damascene trench locations;

etching through said first dielectric layer to said base substrate in areas defined by said patterned mask; and,

stripping said patterned mask from said first dielectric layer defining said first and second damascene trenches.

33. A method of fabricating a semiconductor device according to claim 29, further comprising providing at least one contact implant within said base substrate through said damascene trench.

34. A method of fabricating a semiconductor device according to claim 29, wherein said gate oxide layer formation comprises:

growing an oxide layer on said base substrate;

forming a patterned mask over said semiconductor device, said pattern arranged to expose at least a portion of said oxide layer within said local interconnect areas;

etching away the exposed portion of said oxide layer; and,

stripping said patterned mask from said semiconductor device.

35. A method of fabricating a semiconductor device according to claim 29, wherein said conductive material comprises a polysilicon material.

36. A method of fabricating a semiconductor device according to claim 35, further comprising forming a silicide layer over said polysilicon material within said gate areas and between said polysilicon and said base substrate within said local interconnect areas.

37. A method of fabricating a semiconductor device according to claim 29, further comprising forming lightly doped drain regions in said base substrate after removing said first dielectric layer.

38. A method of fabricating a semiconductor device according to claim 29, further comprising:

forming lightly doped drain regions in said base substrate after removing said first dielectric layer, said lightly doped drain regions formed within said base substrate adjacent to said at least one damascene gate structure and said at least one damascene local interconnect structure;

forming spacers against the vertical walls of said damascene gate structure and said damascene local interconnect structure; and,

forming doped source/drain regions in said base substrate after forming said spacers such that said base substrate is doped more deeply into said base substrate adjacent to said spacers than into said base substrate underneath said spacers.

39. A method of fabricating a semiconductor device comprising:

forming an isolation trench in a base substrate

forming a first dielectric layer over said base substrate;

forming a patterned mask over said first dielectric layer;

etching through said dielectric layer to said base substrate in areas defined by said patterned mask to define a damascene trench in said first dielectric layer, said damascene trench having a gate area and a local interconnect area; and positioned such that at least a portion of said damascene trench at least partially overlies said isolation trench;

stripping said patterned mask from said dielectric layer;

growing an oxide layer on said base substrate, said oxide layer within said gate area of said damascene trench defining a gate oxide layer;

forming a patterned mask over said semiconductor device, said pattern arranged to expose at least a portion of said oxide layer within said local interconnect area;

etching away the exposed portion of said oxide layer within said damascene trench;

providing at least one contact implant within said base substrate through said damascene trench;

stripping said patterned mask from said semiconductor device;

depositing a conductive layer comprising a conductive material over said device such that said conductive layer fills said damascene trench;

planarizing said conductive layer down to the surface of said dielectric layer;

removing said first dielectric layer to define a damascene gate structure and a damascene local interconnect structure;

forming lightly doped drain regions in said base substrate adjacent to said damascene gate structure and said damascene local interconnect structure;

depositing a spacer layer over said device;

anisotropically etching said spacer layer such that spacers are formed over the portions of said base substrate where said lightly doped drain regions are formed; and,

forming doped source/drain regions in said base substrate after forming said

spacers such that said base substrate is doped more deeply into said base substrate adjacent to said spacers than into said base substrate underneath said spacers.

40. A method of fabricating a static memory cell comprising:

forming a plurality of isolation trenches in a base substrate;

forming a first dielectric layer over said base substrate;

forming a first damascene trench having a first gate area, a first local interconnect area, a second gate area, and a second local interconnect area;

forming a second damascene trench having a first gate area, a first local interconnect area, a second gate area, and a second local interconnect area;

forming a gate oxide on said base substrate in said first and second gate areas of both said first and second damascene trenches;

filling said first and second damascene trenches with a conductive material;

removing said first dielectric layer;

doping said base substrate with a first active area between said first gate area of said first damascene trench and said first local interconnect area of said second damascene trench;

doping said base substrate with a second active area between said first local interconnect area of said first damascene trench and said first gate area of said second damascene trench;

doping said base substrate with a third active area between said second gate area of said first damascene trench and said second local interconnect area of said second damascene trench; and,

doping said base substrate with a fourth active area between said second local interconnect area of said first damascene trench and said second gate area of said second damascene trench.

41. A method of fabricating a static memory cell according to claim 40, further comprising providing contact implants before the conductive material is formed within the damascene trenches.

42. A memory device cell layout comprising:

a base substrate;

a first damascene trench formed on said base substrate, said first damascene trench having formed therein, first and second gates and first and second local interconnects;

a second damascene trench formed on said base substrate, said second damascene trench having formed therein, first and second gates and first and second local interconnects;

a first active area between said first gate of said first damascene trench and said first local interconnect of said second damascene trench;

a second active area between said first local interconnect of said first damascene trench and said first gate of said second damascene trench;

a third active area between said second gate of said first damascene trench and said second local interconnect of said second damascene trench; and,

a fourth active area between said second local interconnect of said first damascene trench and said second gate of said second damascene trench.

43. A memory device cell layout according to claim 42, further comprising a fifth active area coupling a first access transistor to said first local interconnect of said second damascene trench and a sixth active area coupling said second local interconnect of said first damascene trench to a second access transistor.

44. A computer system comprising:

a bus;

a central processing unit coupled to said bus;

at least one input-output device coupled to said bus; and,

a memory device coupled to said bus, said memory device having a layout comprising:

a base substrate;

a first damascene trench formed on said base substrate, said first damascene trench having formed therein, first and second gates and first and second local interconnects;

a second damascene trench formed on said base substrate, said second damascene trench having formed therein, first and second gates and first and second local interconnects;

a first active area between said first gate of said first damascene trench and said first local interconnect of said second damascene trench;

a second active area between said first local interconnect of said first damascene trench and said first gate of said second damascene trench;

a third active area between said second gate of said first damascene trench and said second local interconnect of said second damascene trench; and,

a fourth active area between said second local interconnect of said first damascene trench and said second gate of said second damascene trench.